# Silicon nanoelectronics and nanotech innovation

George Bourianoff

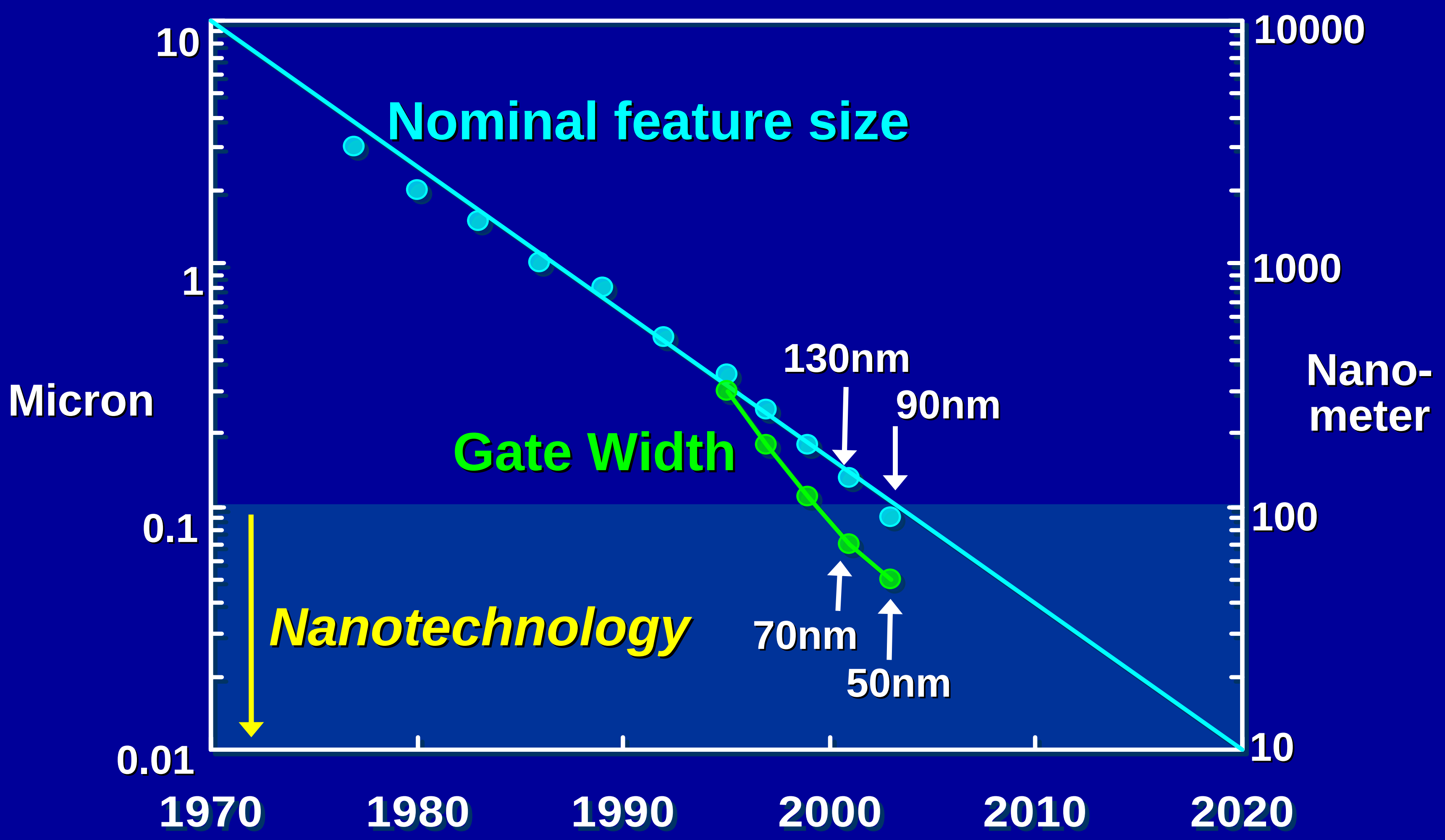
May 26, 2004

Intel Corp

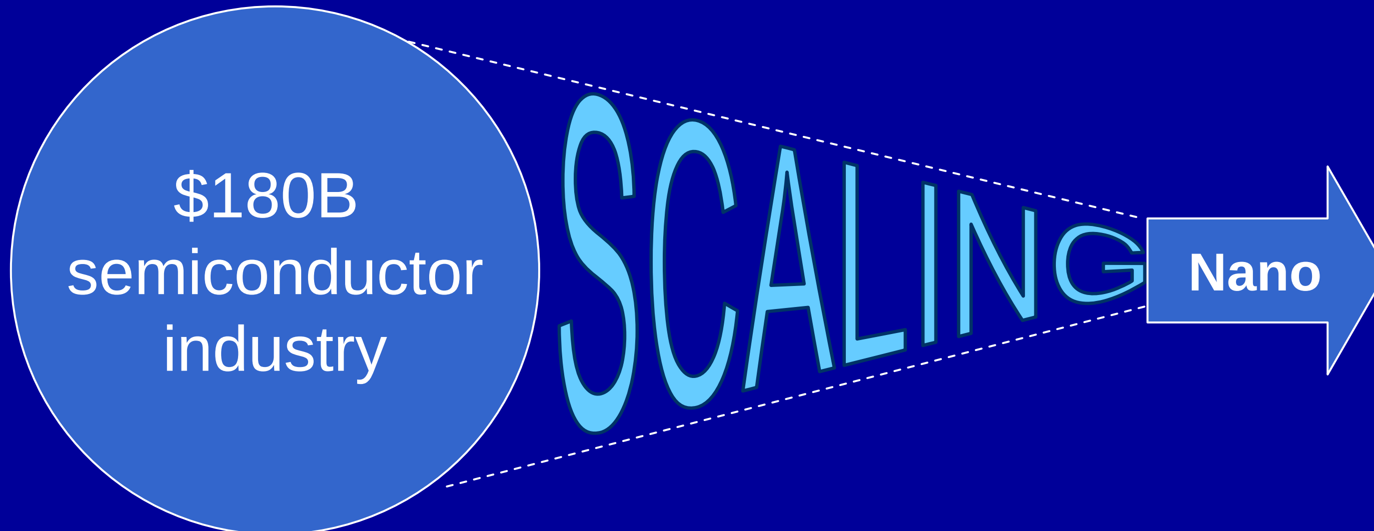
# Key messages

- Extending Moore’s Law
  - enabled by nanotech innovation
- Expanding Moore’s Law
  - The silicon manufacturing infrastructure can enable novel nanotechnology
- Integration of nanotechnology
  - Silicon provides the platform
- Radical new nanotechnologies beyond CMOS will emerge by 2020

# Silicon Nanotechnology is Here!



# Extension of Moore’s Law

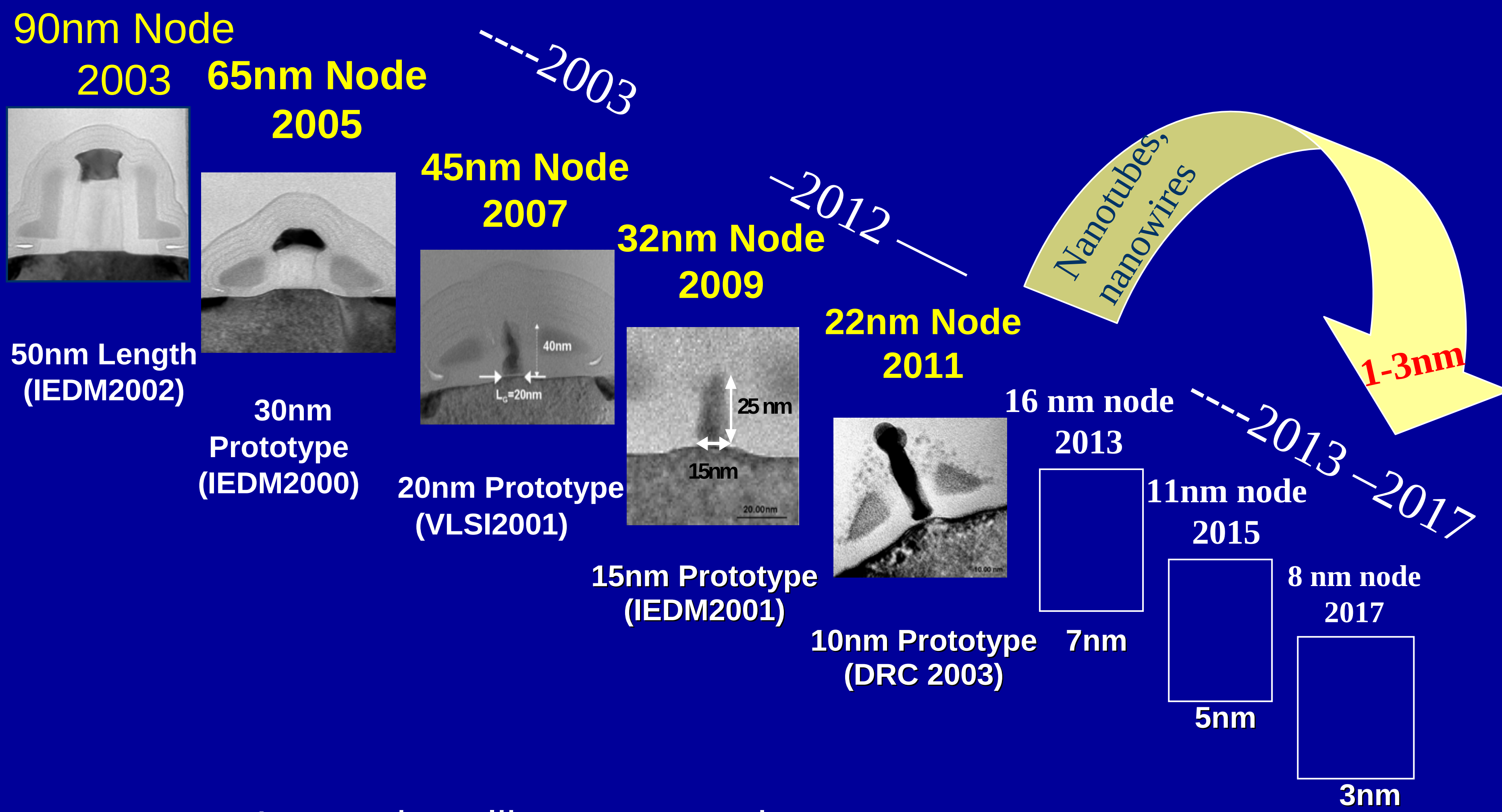



1. Scaling device dimensions downward
2. Scaling wafer diameter upward

| | 1990 | 1995 | 2000 |
|---|---|---|---|
| **DRAMs** | 4 MB | 64 MB | 1 GB |
| **Feature size** | 0.8 µm | 0.35 µm | 0.15 µm |
| **Wafer diameter** | 6” | 8” | 12” |
| **Cost per Megabit** | $6.50 | $3.14 | $0.10 |

Powerful economic engine will drive innovation

# Nanotechnology will extend CMOS scaling

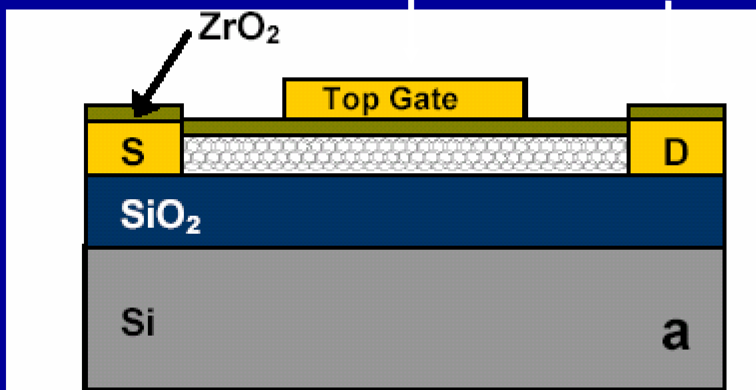


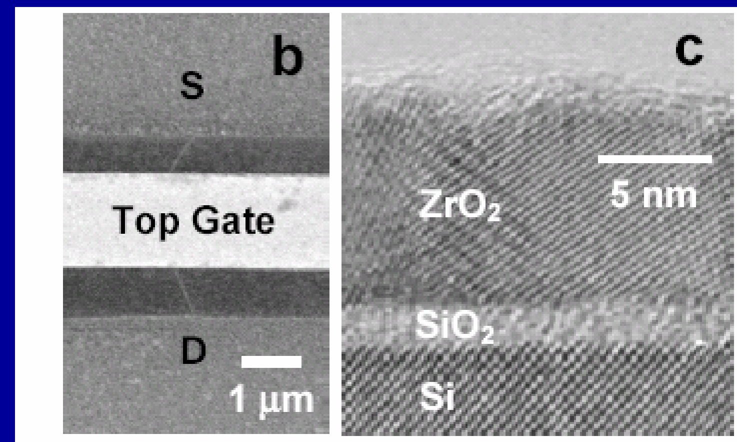

Innovations like quantum dots,
Nanowires, Naotubes, etc.

# Extending CMOS-Nanotubes

E-beam Ti/Au gate

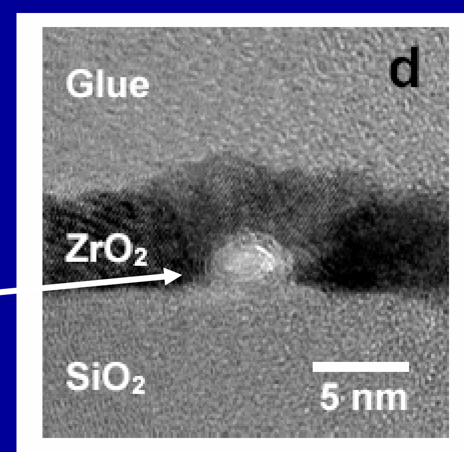
Mo S/D



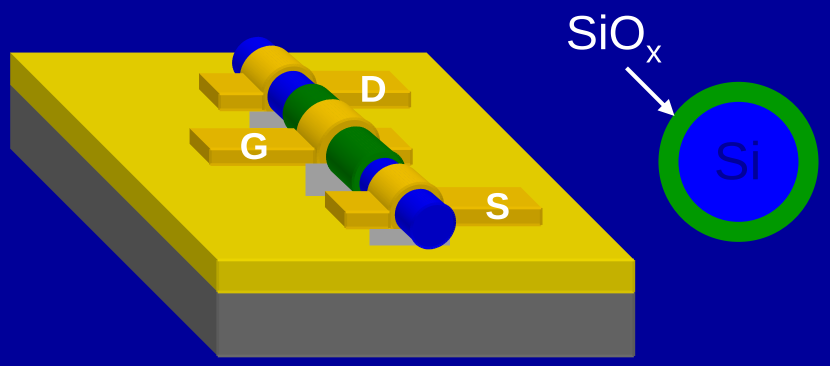

8 nm ZrO2

1.4 nm diameter single wall CNT

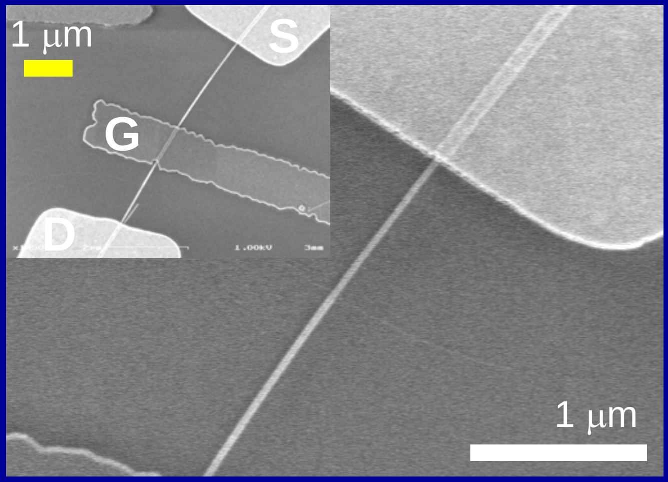


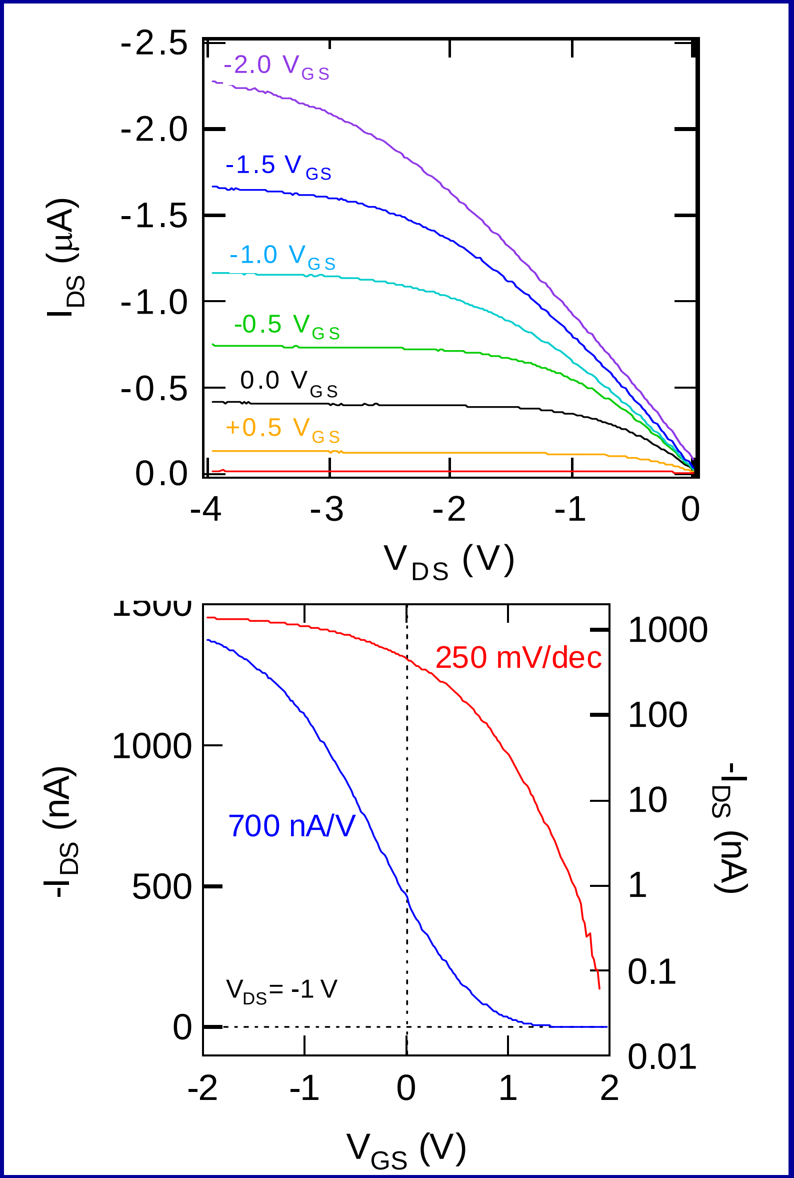

McEuen et. al, . Cornell University

# Extending CMOS - Nanowires

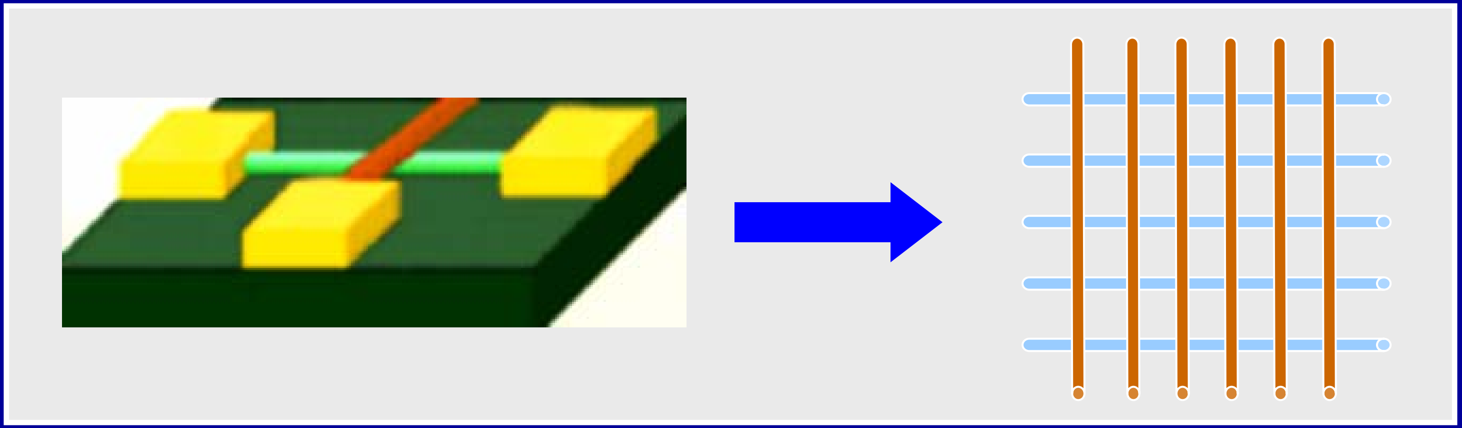



C. Leiber et. al. , Harvard U



# Extending CMOS
# Crossed Nanowire Structures:



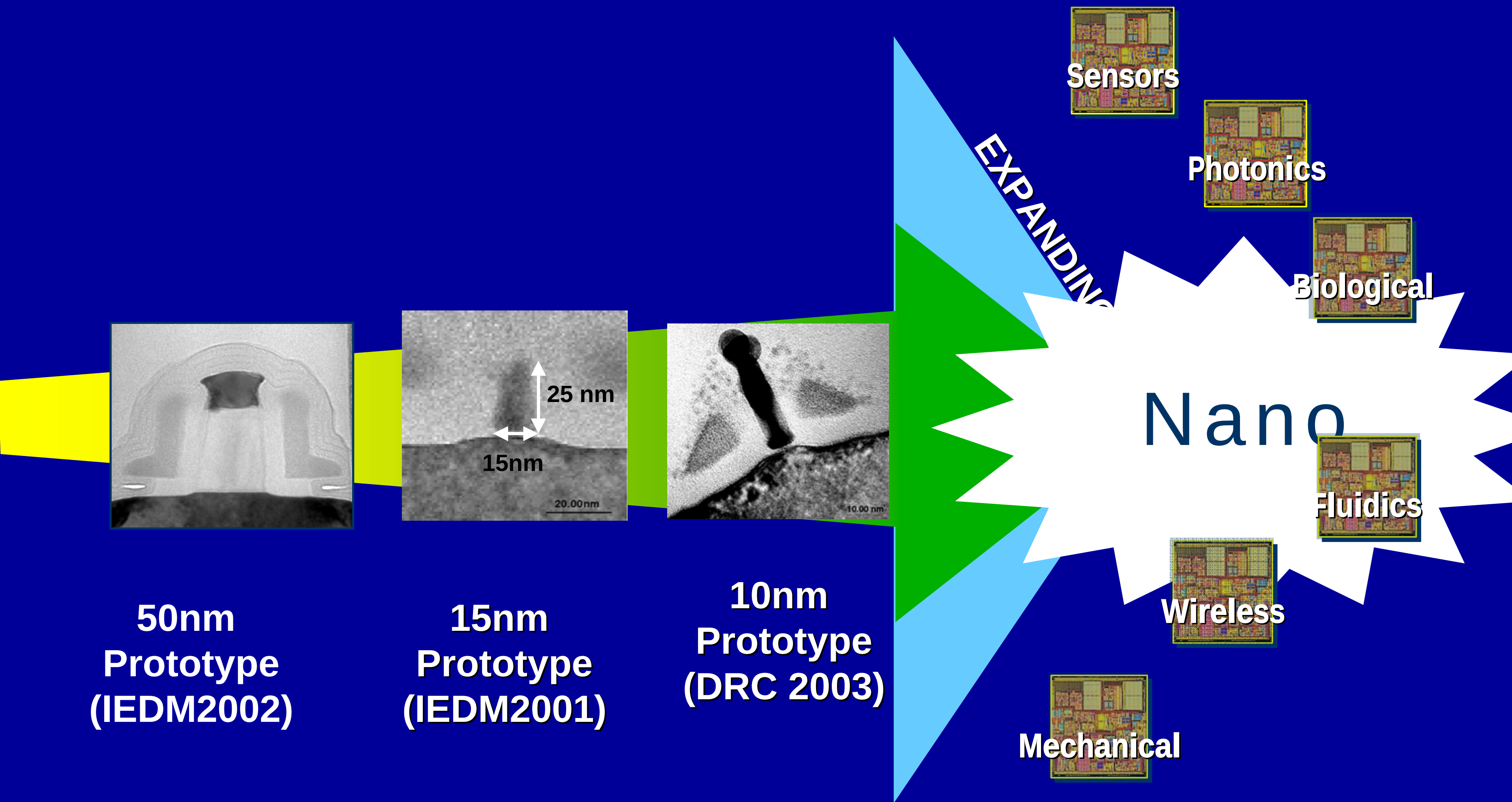
- Nanowires serve dual purpose: both active devices and interconnects.
- All key nanoscale metrics are defined during synthesis and subsequent assembly.
- Crossed nanowire architecture provides natural scaling and potential for integration at highest densities.
- No additional complexity (with added material).

C. Leiber et. al. , Harvard U

# Outline

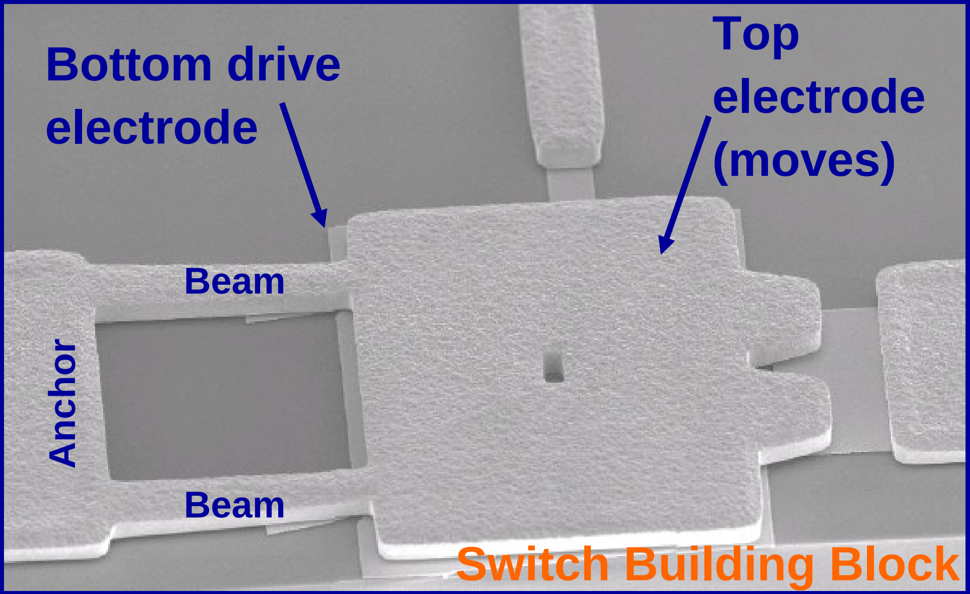
- Extending Moore's Law
  - – enabled by nanotech innovation
- ➢ Expanding Moore's Law
  - – The silicon manufacturing infrastructure can enable novel nanotechnology
- Integration of nanotechnology
  - – Silicon provides the platform
- Radical new nanotechnologies beyond CMOS will emerge by 2020

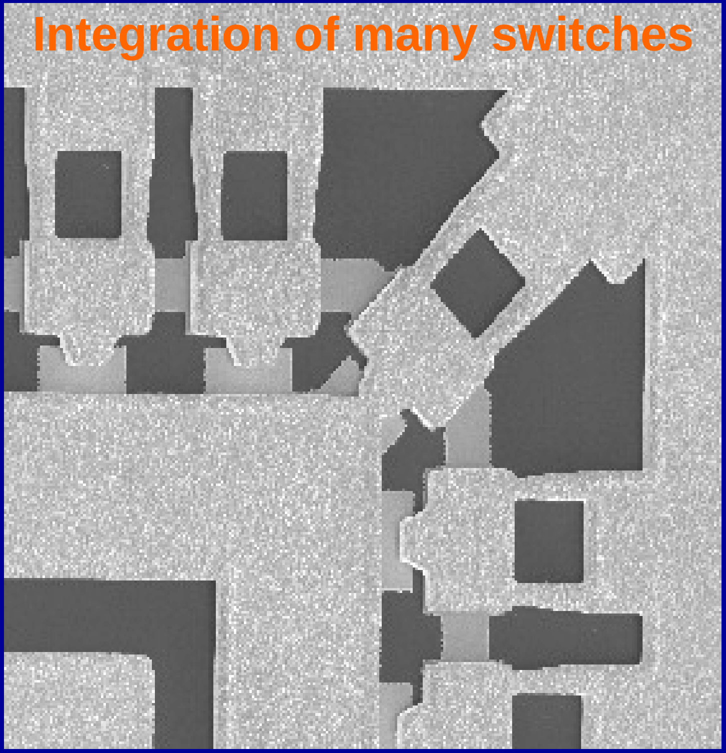
# Expanding Moore's Law

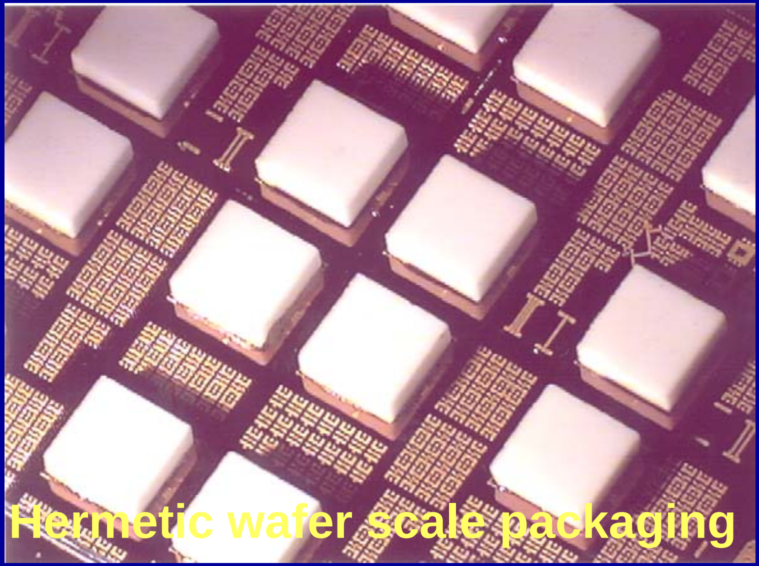



 Silicon manufacturing infrastructure will enable innovation 

# MEMS for RF switching



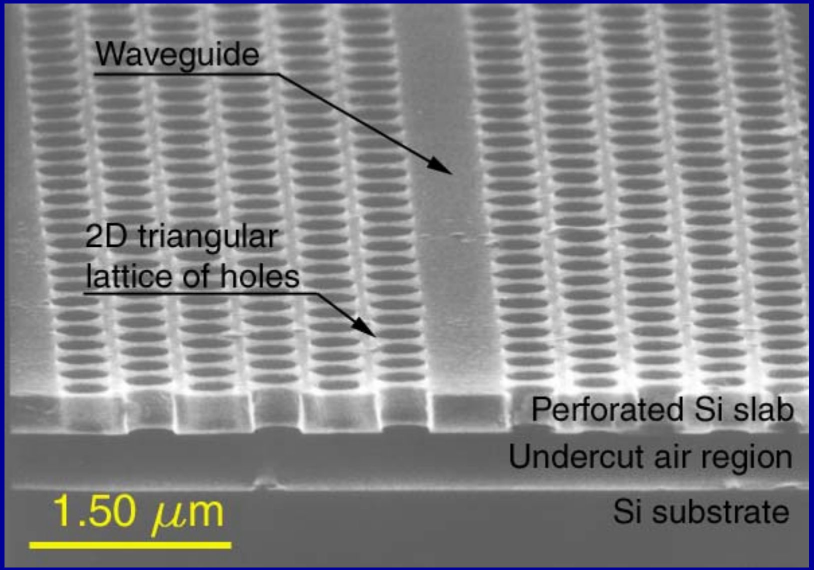




- Laterally lithography requirements are only n-5:
  - Mechanical devices are large10 µm -100 µm
- Vertically:
  - Layer thickness control requirement are extremely stringent: **"Nanometer sized gaps"**
  - Advanced materials with excellent mechanical and electrical properties are needed

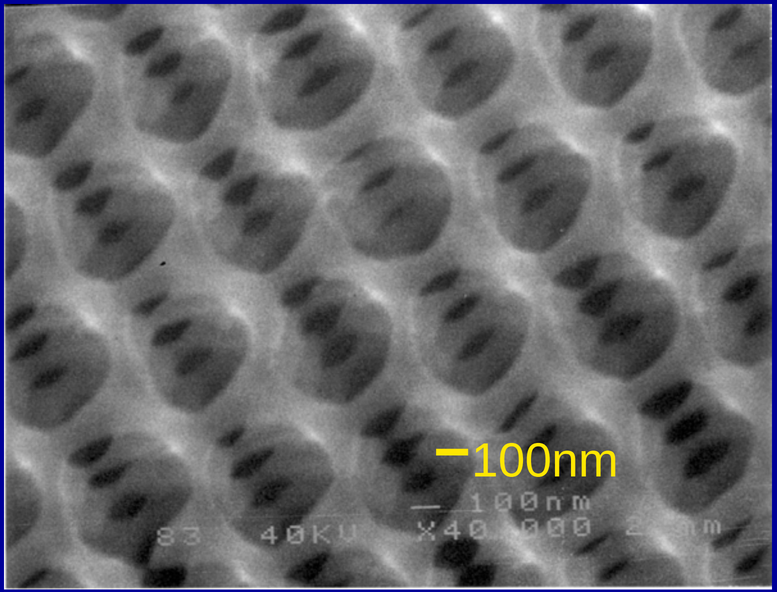
# Photonic crystals

**1D**


**2D**




**3D**




*-Lithography enables Moore's Law scaling*

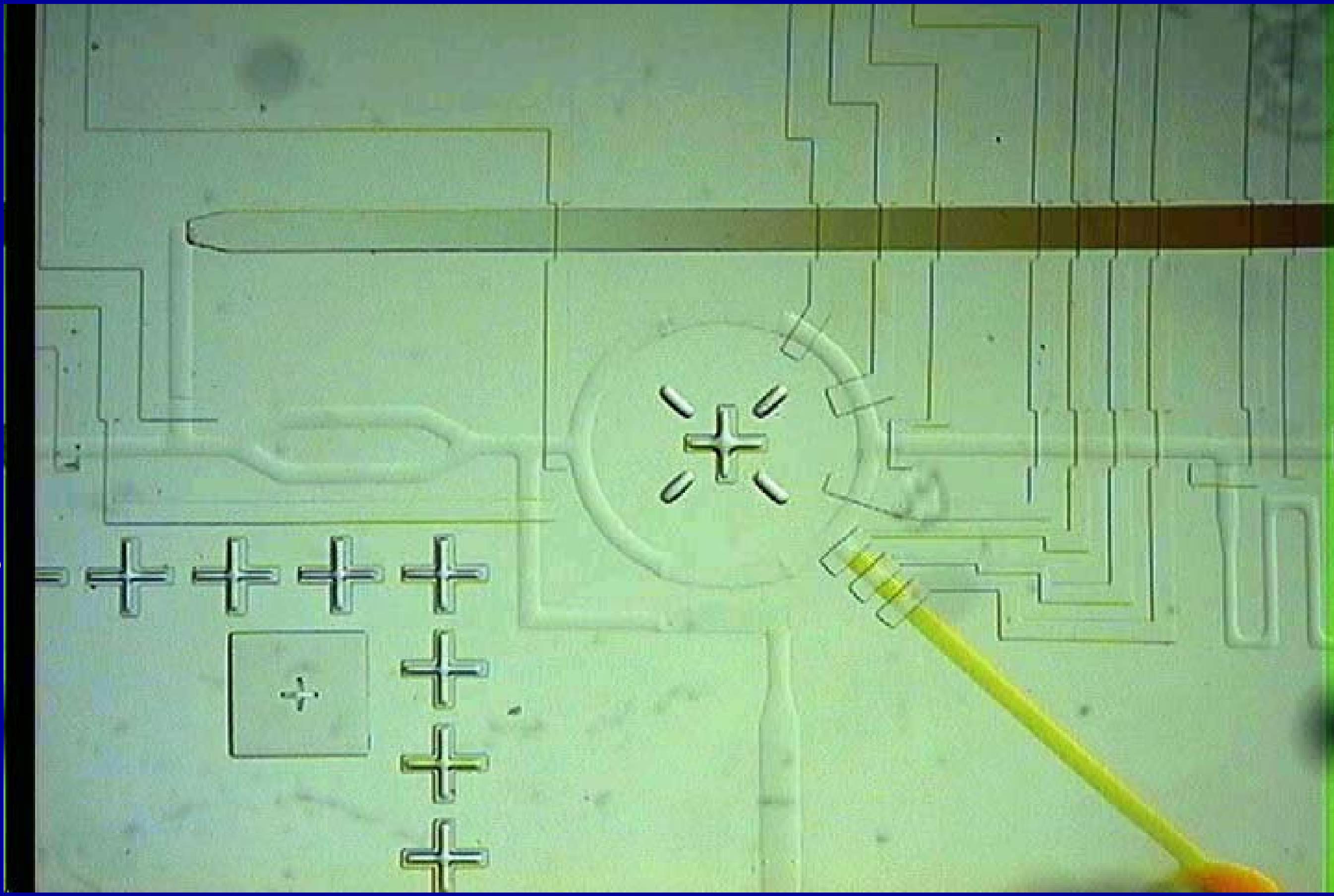


\- *Courtesy, A. Scherer, Caltech*

# Microfluidics

Use silicon technology
To fabricate

- **channels,**
- **Pumps,**
- **valves,**
- **manifolds**
- **reaction chambers**



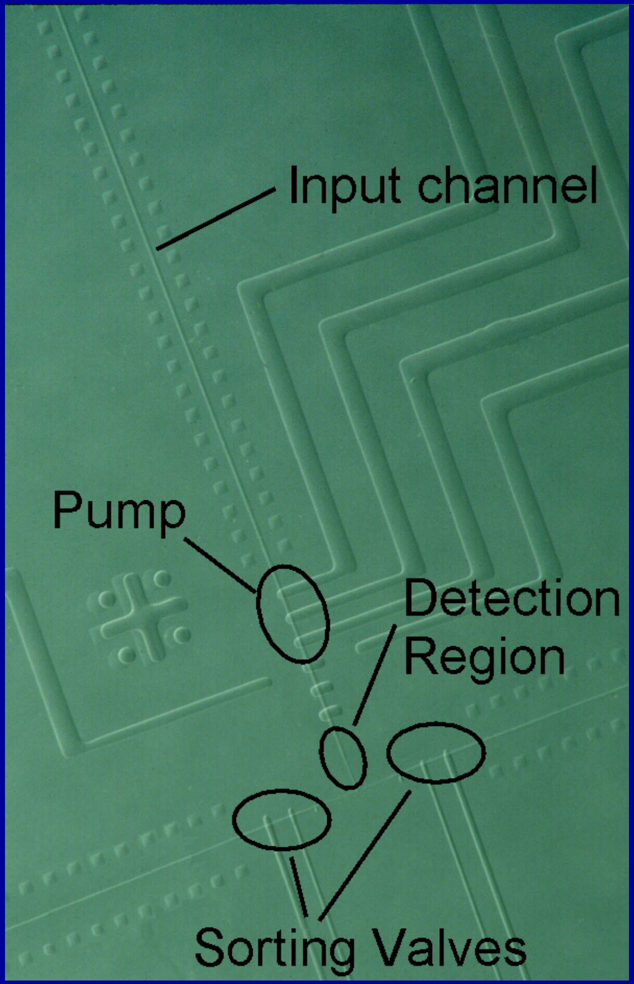


Courtesy A. Scherer, Caltech

# Biological Analysis Systems

*Microfluidic channels can be integrated with electronics and optics for:*

- Compact chemical and biological sensor chips
- “Laboratory on a chip” diagnostic tools
- Short analysis times
- Small analyte volumes






Courtesy, A. Scherer Caltech

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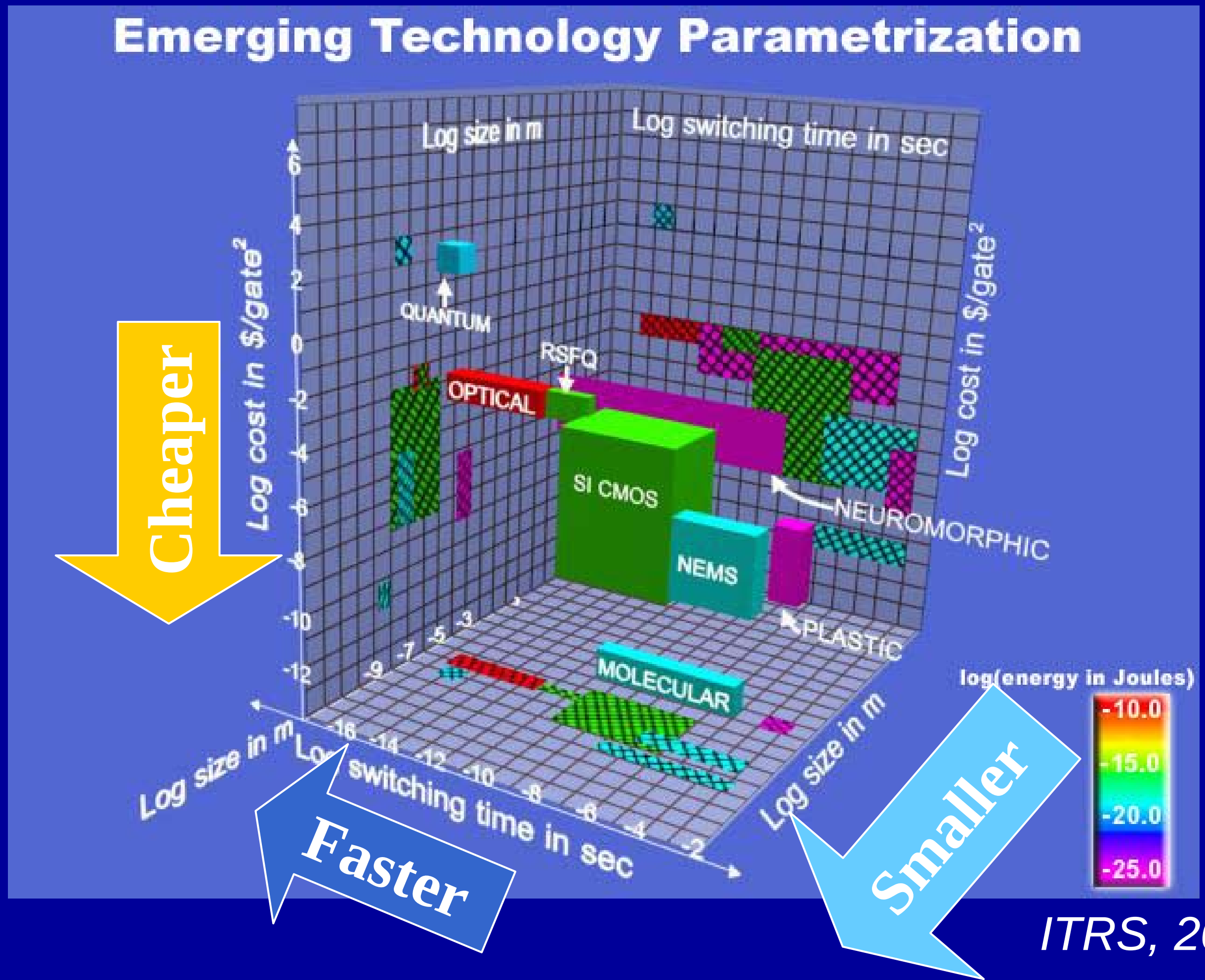
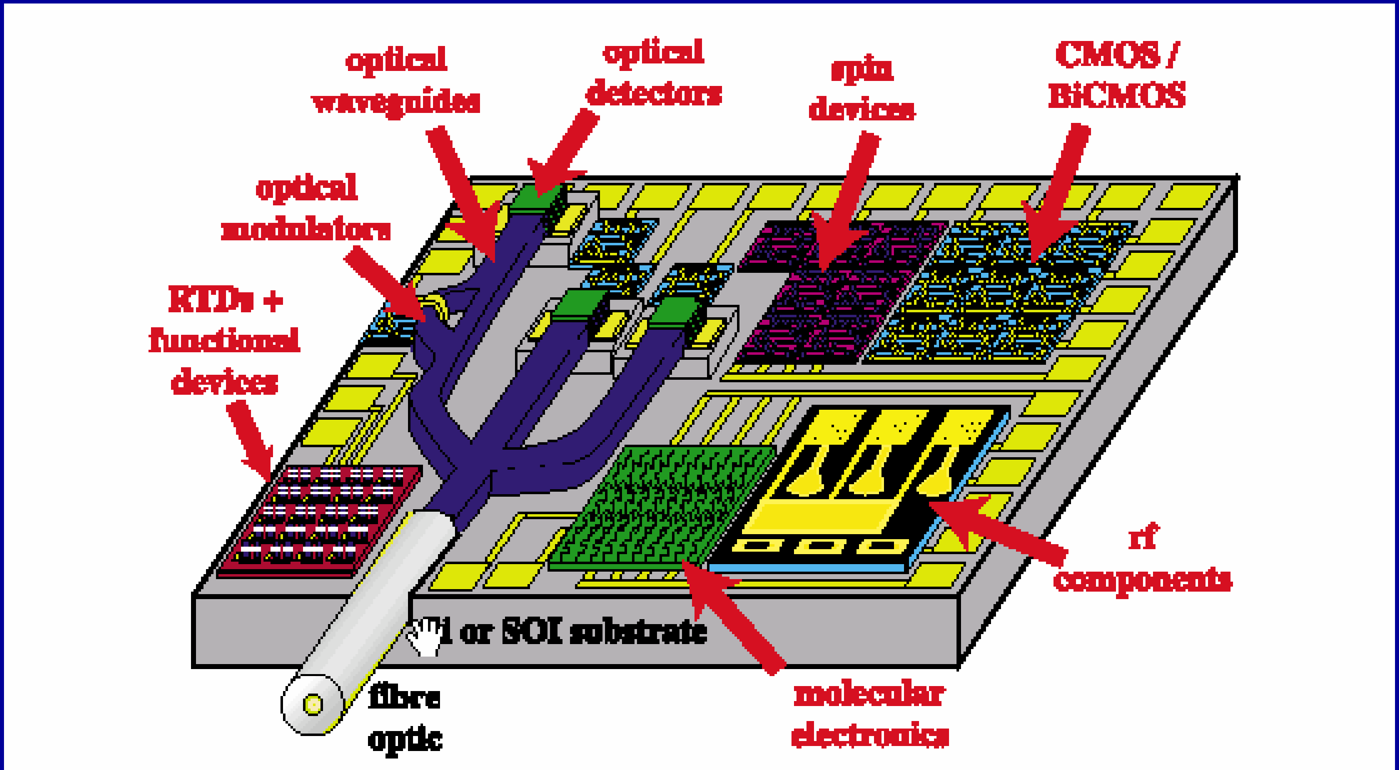
# Radical technologies beyond CMOS




*ITRS, 2001*

***Nothing beats scaled silicon but nanotechnology can complement***

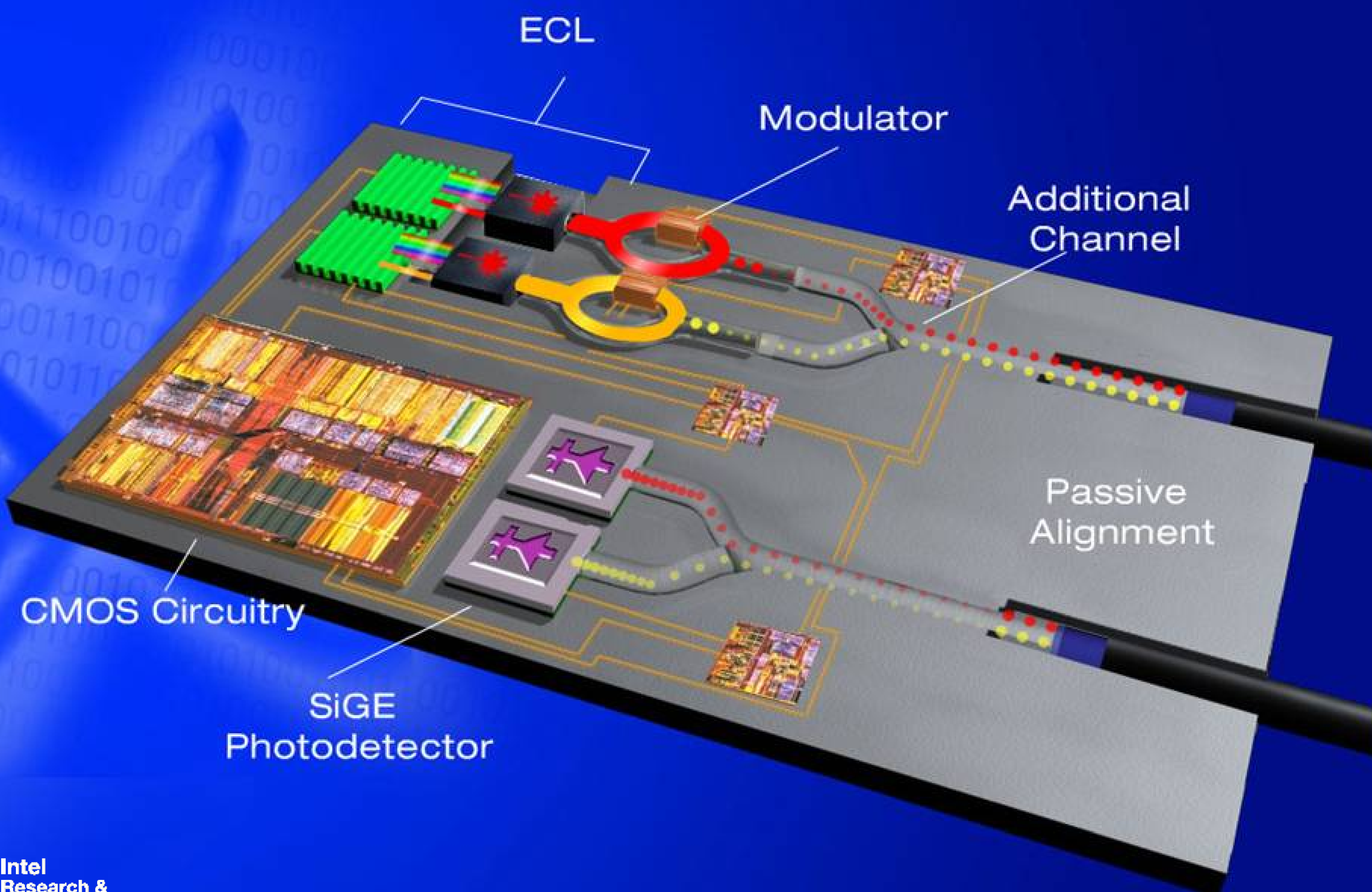
# Heterogeneous integration of alternative technologies*




**European Technology Roadmap for Nanoelectronics*

***Silicon integration platform***

# Silicon Photonics Vision




Intel
Research &
Development

# Anthropomorphic Machines

**Electrical complexity will be very high! The Sony robot depicted has over 40 IC's, tens of sensors, & novel actuation devices (muscles)**

**Innovation is in the integration of Conventional components**

**Sony SDR 4X Robot**
**Dr. Makimoto, IEDM 2002**

**Courtesy, Sony Corporation**

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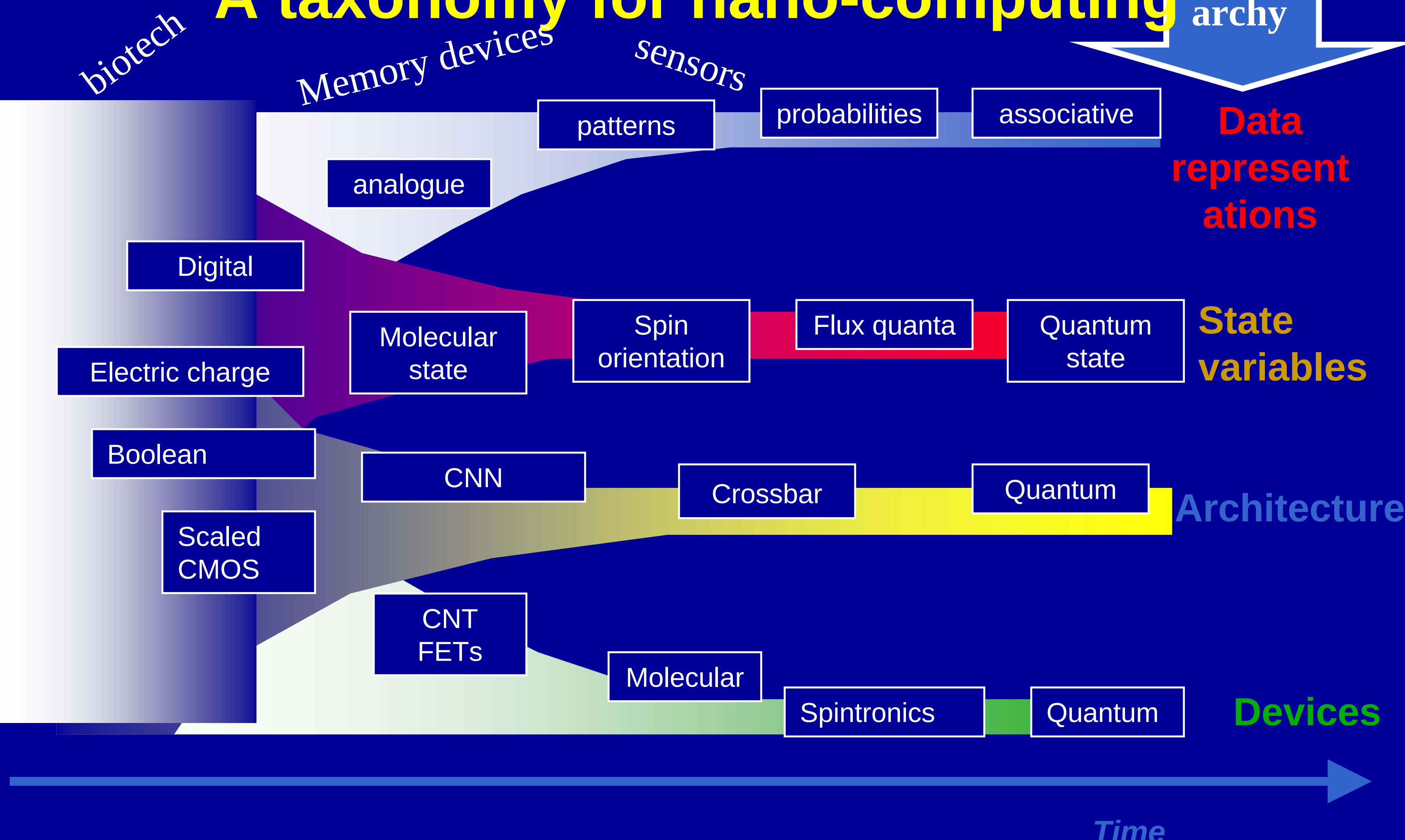
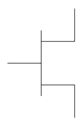
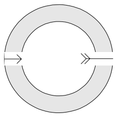
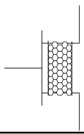
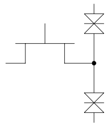
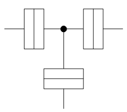
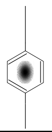
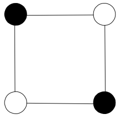
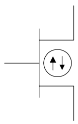
➢ Radical new nanotechnologies beyond CMOS will emerge by 2020

# A taxonomy for nano-computing

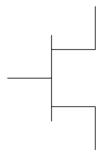
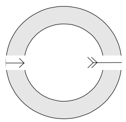
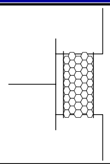
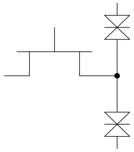
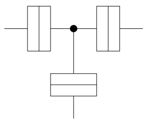
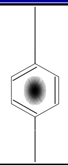
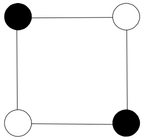
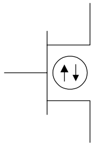



Nanocomputing involves more than nanodevices

# Emerging Research Logic: Projected Parameters ITRS 2003

| *Device* |  |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|---|
| | *FET* | *RSFQ* | *1D structures* | *Resonant Tunneling Devices* | *SET* | *Molecular* | *QCA* | *Spin transistor* |
| *Cell Size* | 100 nm | 0.3 µm | 100 nm | 100 nm | 40 nm | Not known | 60 nm | 100 nm |
| *Density (cm$^{-2}$)* | 3E9 | 1E6 | 3E9 | 3E9 | 6E10 | 1E12 | 3E10 | 3E9 |
| *Switch Speed* | 700 GHz | 1.2 THz | Not known | 1 THz | 1 GHz | Not known | 30 MHz | 700 GHz |
| *Circuit Speed* | 30 GHz | 250–800 GHz | 30 GHz | 30 GHz | 1 GHz | <1 MHz | 1 MHz | 30 GHz |
| *Switching Energy, J* | $2\times10^{-18}$ | $>1.4\times10^{-17}$ | $2\times10^{-18}$ | $>2\times10^{-18}$ | $>1.5\times10^{-17}$ | $1.3\times10^{-16}$ | $>1\times10^{-18}$ | $2\times10^{-18}$ |
| *Binary Throughput, Bit/ns/cm$^2$* | 86 | 0.4 | 86 | 86 | 10 | N/A | 0.06 | 86 |

# Emerging Research Logic: Experimental Demonstrations ITRS 2003

| Device |  |  |  |  |  |  |  |  |
|---|---|---|---|---|---|---|---|---|
| | *FET* | *RSFQ*[J] | *1D Structures* | *Resonant Tunneling Devices* | *SET* | *Molecular* | *QCA* | *Spin transistor* |
| *Cell Size* | 100 nm | 46 μm | 10 μm | 3 μm | 1-100 μm | 120 nm | 5.8 μm | 2 mm |
| *Density ($cm^{-2}$)* | 3E9 | 5E4 | Not known | Not known | Not known | 6E9 | Not known | Not known |
| *Switch Speed* | 700 GHz | 80 GHz | 220 Hz | 700 GHz | 1 MHz | 2 Hz | Not known | Not known |
| *Circuit Speed* | 30 GHz | 20 GHz | Not known | Not known | Not known | Not known | 3 Hz | Not known |
| *Switching Energy, J* | $2\times10^{-18}$ | $>8\times10^{-16}$ | $10^{-10}$ | $10^{-13}$ | $>1.3\times10^{-14}$ | $10^{-9}$ | $>8\times10^{-19}$ | Not known |
| *Binary Throughput Gbit/ns/cm$^2$* | 86 | 9E–4 | Not known | Not known | Not known | 6.4E–9 | Not known | Not known |

# Overall Performance and Risk Assessment Method of Calculation - ITRS 2003

Overall Performance and Risk Assessment (OPRA)

OPRA = Sum [(Performance Potential) x (Risk Assessment)] (Summed over the eight Evaluation Criteria for each Technology Entry)

Maximum (OPRA) = 72

Minimum (OPRA) = 8

# Overall Performance and Risk Assessment for Technology Entries - ITRS 2003

| | |
|---|---|
| *Potential for the Technology Entry is projected to be significantly better than silicon CMOS (compared using the Technology Evaluation Criteria) and solutions to accomplish the most of the Technology Evaluation Criteria are known resulting in lowest risk (OPRA $\geq$ 50)* | ***Potential/ Risk*** |
| *Potential for the Technology Entry is projected to be comparable to or slightly less than silicon CMOS (compared using the Technology Evaluation Criteria) and concepts to accomplish most of the Technology Evaluation Criteria have been proposed and are judged to be of moderate risk (OPRA = 40 – 49)* | ***Potential/ Risk*** |
| *Potential for the Technology Entry is projected to be comparable to or less than silicon CMOS (compared using the Technology Evaluation Criteria) and concepts to accomplish a few of the Technology Evaluation Criteria have been proposed and are judged to be of higher risk (OPRA = 30 – 39)* | ***Potential/ Risk*** |
| *Potential for the Technology Entry is projected to be significantly less than silicon CMOS (compared using the Technology Evaluation Criteria) and no solutions or concepts have been proposed accomplish most of the Technology Evaluation Criteria and are judged to be of highest risk (OPRA < 30)* | ***Potential/ Risk*** |

# Technology Performance and Risk Evaluation Emerging Research Memory Devices -ITRS 2003

## Potential/Risk

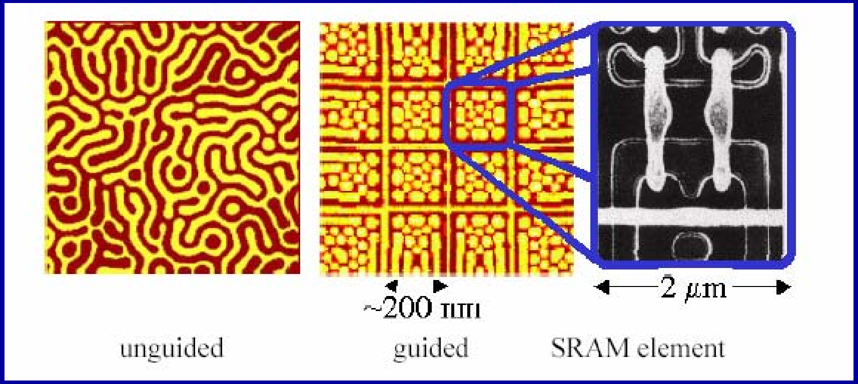
| *Memory Device Technologies* | *Performance [A]* | *Architecture compatible [B]** | *Stability and reliability [C]* | *CMOS compatible [D]*** | *Operate temp [E]**** | *Energy efficiency [F]* | *Sensitivity Δ(parameter) [G]* | *Scalability [H]* |
|---|---|---|---|---|---|---|---|---|
| *Floating Body DRAM* | **2.3/2.3** | **3.0/3.0** | **2.0/2.7** | **3.0/3.0** | **3.0/3.0** | **2.0/3.0** | **2.3/2.9** | **2.8/2.7** |
| *Phase Change Memory* | **2.6/2.9** | **2.2/3.0** | **2.3/2.2** | **2.2/3.0** | **3.0/3.0** | **1.8/2.7** | **2.1/2.1** | **2.7/2.2** |
| *Nano-floating Gate Memory* | **3.0/2.2** | **2.9/3.0** | **2.0/2.7** | **3.0/3.0** | **3.0/3.0** | **2.1/2.8** | **1.6/2.0** | **2.4/2.0** |
| *Insulator Resistance Change Memory* | **2.4/2.1** | **2.7/2.7** | **2.2/2.4** | **2.1/2.8** | **3.0/2.9** | **2.8/2.0** | **2.1/2.0** | **2.7/2.4** |
| *Molecular Memory* | **1.6/1.2** | **1.8/2.0** | **1.8/1.4** | **1.9/2.1** | **2.8/2.3** | **2.3/1.9** | **2.1/1.7** | **2.6/2.2** |
| *Single/Few Electron Memory* | **1.1/1.3** | **1.9/1.3** | **1.1/1.0** | **2.4/1.9** | **1.3/1.3** | **2.4/1.2** | **1.3/1.0** | **2.6/1.4** |

# Technology Performance and Risk Evaluation Emerging Research Logic Devices –ITRS 2003

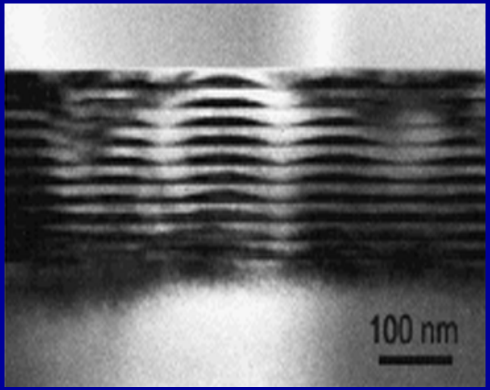
## Potential/Risk

| *Logic Device Technologies* | *Performance [A]* | *Architecture compatible [B]** | *Stability and reliability [C]* | *CMOS compatible [D]*** | *Operate temp [E]**** | *Energy efficiency [F]* | *Sensitivity Δ(parameter) [G]* | *Scalability [H]* |
|---|---|---|---|---|---|---|---|---|
| *1D Structures* | **2.3/2.2** | **2.2/2.9** | **1.9/1.2** | **2.3/2.4** | **2.9/2.9** | **2.6/2.1** | **2.6/2.1** | **2.3/1.6** |
| *RSFQ Devices* | **2.7/3.0** | **1.9/2.7** | **2.2/2.8** | **1.6/2.2** | **1.1/2.7** | **1.6/2.3** | **1.9/2.8** | **1.0/2.1** |
| *Resonant Tunneling Devices* | **2.6/2.0** | **2.1/2.2** | **2.0/1.4** | **2.3/2.2** | **2.2/2.4** | **2.4/2.1** | **1.4/1.4** | **2.0/2.0** |
| *Molecular Devices* | **1.7/1.3** | **1.8/1.4** | **1.6/1.4** | **2.0/1.6** | **2.3/2.4** | **2.6/1.3** | **2.0/1.4** | **2.6/1.3** |
| *Spin Transistor* | **2.2/1.7** | **1.7/1.6** | **1.7/1.7** | **1.9/1.4** | **1.6/2.0** | **2.3/2.1** | **1.4/1.7** | **2.0/1.4** |
| *SETs* | **1.1/1.2** | **1.7/1.2** | **1.3/1.1** | **2.1/1.4** | **1.2/1.8** | **2.6/2.0** | **1.0/1.0** | **2.1/1.7** |
| *QCA Devices* | **1.4/1.3** | **1.2/1.1** | **1.7/1.8** | **1.4/1.6** | **1.2/1.4** | **2.4/1.7** | **1.6/1.1** | **2.0/1.4** |

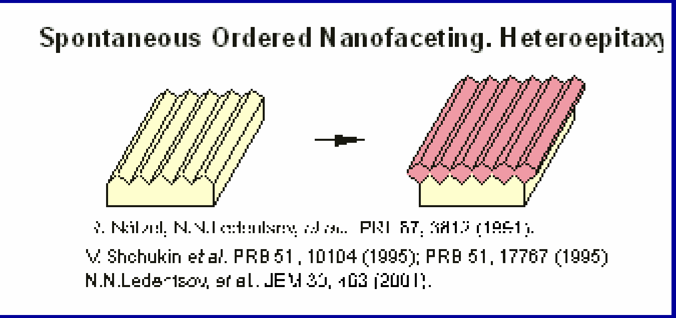
# Assisted self assembly

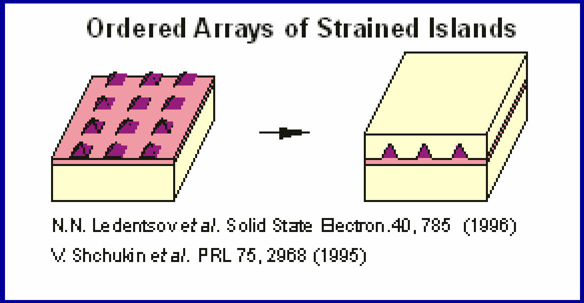



Templated phase separations – Z. Suo, W. Lu J. Nanoparticle Research 2001




3D Self aligned SiGe nanostructures. L. Tsybeskov, NJIT

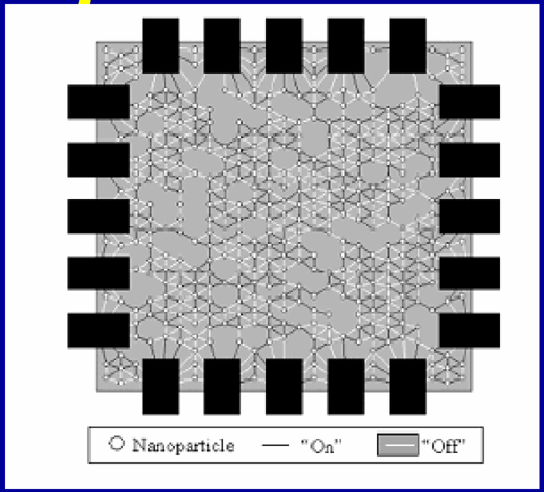


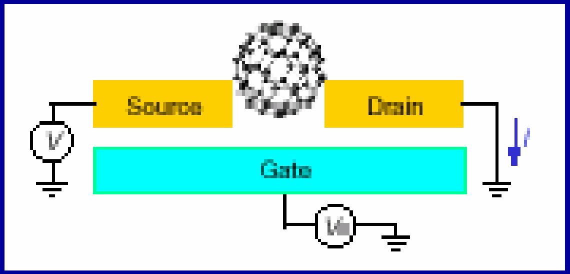

Crystallographic strain field nanostructure formation

# Molecular logic

- 2D self assembled arrays*
  - Nanoparticles connected by programmable molecules
  - No gain, slow
  - * J. M. Tour et. al Rice



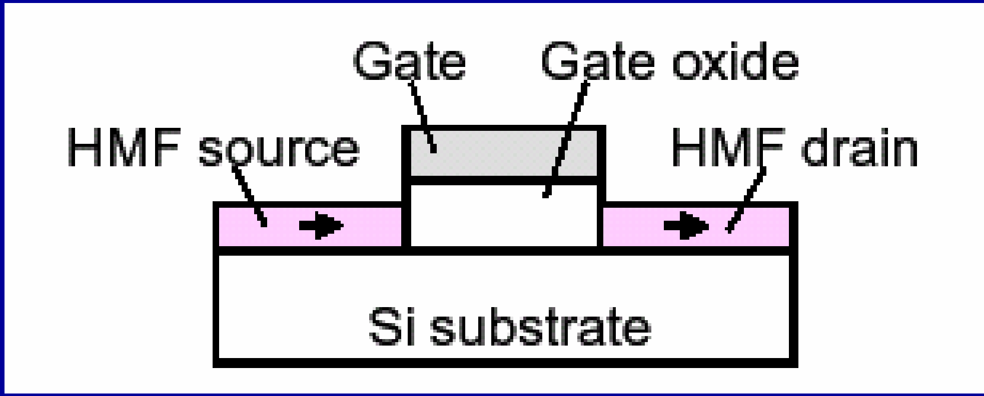

- Back gated 3 terminal devices
  - Molecule acts as channel
  - No gain, very low current, slow McEuen et.al. Cornell




***Very early stage research – contacts are critical***

# Spin MOSFET devices

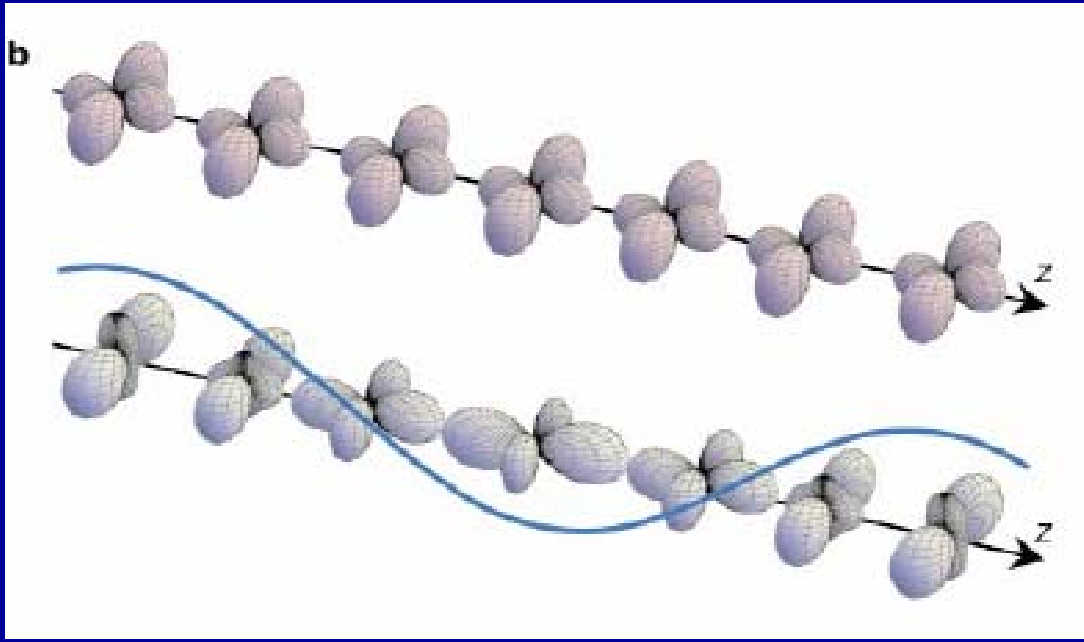
- Spin modulated current flow
  - High Ion/Ioff
  - High gain
- Half Metal source – drain
- Requires 100% spin polarized injection




Sugahara and Tanaka, Applied Physics Letters, Vol 84, No 13, Mar 29, 2004

# Coherent states in condensed matter

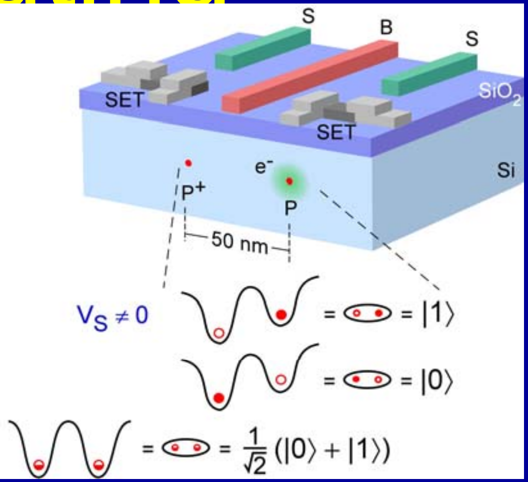
- Strongly correlated electrons in $LaMnO_3$
- Ultra fast $<10^{-12}$ sec
- Tc ~ 140 K

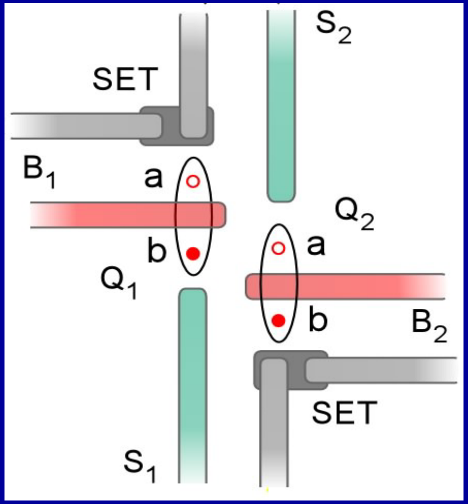


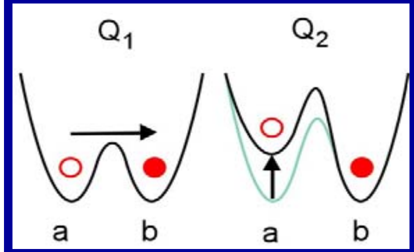

E. Saitoh et.al, Nature, Vol 410. Mar 8, 2001

# Quantum computing

- Utilizes single phosphorous atoms implanted in silicon
- Gate electrodes control entanglement of the wavefunctions
- Qubit spacing of order 30 nm
- Quantum error correction difficult - 6 correction bits per single information bit
- Single logical qubit not yet demonstrated
- Large, well organized program in Australia




***Most speculative of alternative logic***

# Putting the pieces together – Functionally organized materials*

Functionally Organized materials

- Near field energy transfer
- Alternative architectures And data structures
- Alternative state variables
- Crystallographic Self assembly
- Femptosec, nanometer interactions
- CMOS process compatibility
- Plasmonics
- Non equilibrium systems

*ITRS Emerging Research Device Workshop, Stresa Italy, 2004

# Definitions

- Functionally organized materials*
  - Material systems which enable distributed and interacting device functionalities in order to store and manipulate computational state arrays
- Metacrystals
  - 3D super lattices of interacting quantum dots, nanocrystals, phonons and plasmons

*Emerging Research Materials Working Group – ITRS 2004

# Conclusions

- Nanotech innovation can help Extend Moore's Law
- Silicon manufacturing infrastructure can help expanding Moore's Law
- Silicon provides the ideal platform for heterogeneous Integration of nanotechnology
- Radical new nanotechnologies will emerge by 2020
- Worldwide research and innovation needed

For further information on Intel's silicon technology,

please visit the Silicon Showcase at

www.intel.com/research/silicon

# Nanocrystals give added functionality

•flash memories with Si quantum-dot array floating gate

•All optical memory devices